

REMARKS

The present application contains claims 1-19 and 21-28. Claim 20 has been cancelled. Claim 20 was objected to because of an extraneous word. In claims 21, 22 and 28, which have been put into independent claim the extraneous word has been omitted, a cosmetic change.

Claims 1, 2, 11, 12 and 21 stand rejected and claims 3-10, 13-19 and 22-28 are objected to. Claims 21, 22 and 28 have been put into independent form. Claim 20 has been cancelled.

Claims 1, 2, 11, 12, 20 and 21 stand rejected under 35 U.S.C. §102(a) as being anticipated by Monnet, et al. (US Patent 6,465,790). Applicants respectfully traverse the rejection and submit that the Monnet patent does not provide a *prima facie* case for anticipation.

This group of claims contains independent claims 1, 12 and 21.

Claim 1 contains the limitation that "said processing circuits are mounted on said printed circuit board at locations remote from said detectors." Monnet does not meet the requirements of claim 1 for at least two reasons. As is clear from col. 4, lines 18-24, the detectors are mounted on substrate 5 and not on substrate 6 as indicated in the second paragraph of item 4 of the office action. The processing circuits (10c) are mounted on substrate 6 (col. 4, lines 30-32). Thus, the circuits and detectors of Monnet are *not* mounted on a same substrate as alleged by the Examiner.

Furthermore, the ASIC 10c of Monnet is not only not mounted on the same circuit board, it is not remote from the detectors. Rather it is immediately behind the detectors on the back side of substrate 6. Based on the sizes of components shown, the distance between the ASIC and the back of the detectors is at most a very few mm, hardly meeting any definition of "remote."

Applicants submit that either of these differences is sufficient to avoid anticipation of claim 1 by Monnet.

Claim 12 contains the limitation of "locating said processing circuits so that they are remotely situated with respect to said pixelated detector." As indicated above, with respect to claim 1, the ASIC of Monnet is not remote from the detectors.

Claim 21 requires that the processing circuits and the pixelated detectors are on separate printed circuit boards. Claim 21 additionally requires that the boards be connected via sockets in one of the boards. However, the Figs. of Monnet do not show any sockets on either elements 5 or 6. Rather, there appear to be unnumbered landings on at least element 6 which mate with similar landings on element 5 to form a slight spacing between them for ground plane 5, which

one assumes has cut-outs from the landings. Applicants submit that the use of sockets *within* the structure shown in Monnet would run counter to the obvious attempt to reduce the size of the device.

Claims 1 and 12 stand rejected under 35 U.S.C. §102(a) as being anticipated by Mestais et al. (US Patent 6,365,900). Applicants respectfully traverse the rejection and submit that these claims are not *prima facie* anticipated by Mestais.


The Mestais patent describes the construction as follows:

"Furthermore, detectors 42 are located on printed circuit board 46 and are connected to preamplifiers (not shown) on this board. Board 46 *collects detection signals from the various individual detectors, shapes them and then sends them to a* calculation and information processing unit 48. This unit calculates position and energy of events."

It is quite clear from this discussion that the signal processing of the detected signals takes place on the board on which the detectors is mounted. Furthermore, when noting the position of calculation and information processing circuit as being immediately behind the detectors, and the fact that the detectors cover the entire area of the printed circuit board, the processing circuits are not remote from the detectors as required by claims 1 and 12.

In view of the above amendments and arguments, applicants submit that the application is in order for allowance. Notice to that effect is respectfully solicited.

Respectfully submitted,
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